Space Critical Technologies for EU Non-Dependence

Technical Guidance Document of Horizon Europe Space Work Programme 2025

Applicable to:

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Table of Acronyms

AI	Artificial Intelligence
BOL	Beginning Of Life
CPT	Coherent Population Trapping
CSAC	Chips Scale Atomic Clock
EO	Earth Observation
EOL	End of Life
FPGA	Field Programmable Gate Array
HSSL	High Speed Serial Link
JTF	Joint-Task-Force
LEO	Low Earth Orbit
LET	Linear Energy Transfer
MRAM	Magnetic Random Access Memory
N7	Technology Node 7nm
R&D	Research and Development
SEE	Single Event Effect
SiP	System in Package
TID	Total Ionizing Dose
TRL	Technology Readiness Level
TRNG	True Random Number Generator
TSN	Time-Sensitive Networking
UDSM	Ultra Deep Sub Micron

1 INTRODUCTION

In the 2019 political guidelines, the European Commission President von der Leyen underlined that “it is not too late for Europe to achieve technological sovereignty in some critical technology areas”.
The 2020 EU industrial strategy stated: “Europe’s strategic autonomy is about reducing dependence on others for things we need the most: critical materials and technologies, food, infrastructure, security and strategic areas such as Space. They also provide Europe’s industry with an opportunity to develop its own markets, products and services which boost competitiveness.”

In 2021, the European Commission has established the EU Observatory of Critical Technologies (OCT) tasked with the objective of identifying, mapping critical space and defence technologies and drafting related EU technology roadmaps. So far the OCT has produced a number of classified documents related to different space and defence technologies and, since 2025 also EU technology roadmaps. Information stemming from the OCT is informing this Technical Guidance Document.

The EU is therefore supporting the development of critical space technologies that are strategically important for Europe.

The expected developments listed in this document are identified by the European Commission and respond to specific needs of EU Space missions (e.g. Galileo, Copernicus, EGNOS, IRIS²…).

2 DEFINITION OF NON-DEPENDENCE

In the context of this document, it is important to recall the definitions of “Independence” and of “Non-Dependence”, namely:

- “Independence” would imply that all needed space technologies are developed in Europe.

- “Non-dependence” refers to the possibility for Europe to have free, unrestricted access to any required space technology.

In particular, the following are criteria used to evaluate if a technology is considered to be part of the list of critical space technologies:

1. Items shall be of low integration level, i.e. building blocks and components (System/sub-system assembly are not included)
2. Items shall have a clearly identified function and performance target
3. Items shall be multi use and/or applications (i.e. not an enabling technology for a one-shot use)

4. Items shall be not available from a European source and for which the unrestricted availability from non-European suppliers cannot be assured
5. Critical items for which no adequate or sufficient action is on going

2.1 Technology Readiness Level

The reference TRL definition is the ISO Standard 16290 “Definition of Technology Readiness Levels (TRLs) and their criteria of assessment”.

3 Space Critical EEE Components for EU non-dependence

3.1 EEE Components

3.1.1 MICROPROCESSORS

Expected Technology Development	This action should pave the way for the development of the next EU based rad-hard space compatible microprocessor, based on 7nm FinFet technology.
	
	The development should be based on a test chip approach. Test chips of incremental complexity is required before the final, full microprocessor product tape out.
	
	This activity will cover the design of specific functionalities, integrated IP cores, tape out and testing (in a representative environment). The number of test chips will depend on the silicon area of each test chip.
	
	The final 7nm space microprocessor is expected to meet the following requirements:
	• 8-cores, 64-bit at 2GHz, fault-tolerant, RISC-V architecture
	• Radiation robustness:
	    o SEE immunity up to LET 62 MeV*cm2 /mg,
	    o TID > 100 Krad (target 150 Krad)
	• Security features:
	    o Secure enclave, Boot and Platform Root of Trust
	    o Embedded TRNG function
	    o Support for post-quantum cryptography
	• Vector Processing Unit
	• AI Accelerator on-chip
	• Memory interface:
	    o DDR4/5 and LPDDR5x memory controller with PHY
	• High Speed Serial Link (HSSL) of at least 1Gbps with implementation of error detection and correction mechanisms
	• Integrated System Controller
	• TSN Ethernet Switch
	
	During the first few months of the project a market and requirement analysis, with primarily focus on relevant EU space missions (e.g. Galileo, EGNOS, Copernicus, SST, IRIS^2) in a form of deliverable should be planned. The content will be used for confirming, discussing and/or tuning the requirements.

	The preferable approach should support a chiplet based architecture. Therefore, the exploitation of current on-going developments of the next EU FPGA on 7nm is encouraged. Moreover, it is suggested to analyse the necessary interfaces and their requirements, in terms of interoperability, speed, latency, within the course of this activity. In this context, a die to die (D2D) interconnect should be evaluated under the light of benefits in terms of low latency and high bandwidth. The activity should potentially consider also relevant IPs developed under on-going activities at EU level or available on the market. This later option is expected to be justified and it is subject to approval by the granting authority. It is anyway mandatory that security related features shall be developed or provided by suppliers in line with the eligibility conditions of the topic.
Estimated Initial TRL:	3
Target TRL	5
Applicable Mission Class(es)	SatCom, EO and Navigation
Remarks / Notes	The reference TRL definition is the ISO Standard 16290.

3.1.2 MEMORIES

Expected Technology Development	This action should support the industrialization of EU based MRAM non-volatile memories for space applications. At the end of the activity an EU based MRAM non-volatile memory with a capacity of at least 1024Mb will be made available on the market accommodating needs for:
	- configuration and program storage
	- mass memory data storage applications
	
	The industrialized memory should meet the following requirements:
	- Radiation robustness:
	  o TID > 100 krad Si
	  o SEL LET > 85 MeV.cm²/mg
	
	- Operating temperature: -55 °C to +125 °C
	- Compatibility with EU FPGAs such as NG-ULTRA, NG-ULTRA300 including their booting

	The development is expected to focus on the industrialization of MRAM non-volatile memories with 512 Mb and 1 Gb memory density. Therefore, the industrialization should be based on already existing design and manufactured prototype demonstrating electrical performance and space compatibility as per the given requirements. As this development aims at covering the industrialization phase, the design and production of the memory should avoid a MPW approach and pursue a full reticle maskset. The memory shall be compatible with future complex components as for example the next EU FPGA and/or Microprocessors based on 7nm. Dedicated activities foreseen for the completion of the product shall be included. Those include for example assembly, packaging, electrical, functional characterization. The product is expected to undergo a full space qualification.
Estimated Initial TRL:	5
Target TRL	8
Applicable Mission Class(es)	SatCom, EO and Navigation
Remarks / Notes	The reference TRL definition is the ISO Standard 16290. As this development is expected to achieve a full space qualification, applicants are reminded that the Work Programme has specific provisions that must be satisfied (e.g. submission of the qualification data pack to the granting authority, EU flag engraving on the package)

3.1.3 CONNECTORS

Expected Technology Development	This development aims at building capabilities in the EU for manufacturing and supply of space qualified connectors. Four types of connectors are identified as a priority in the context of EU space non-dependence. The project should cover the development of all four types of connectors unless duly justified. The development should cover the following connectors: 1) Circular high voltage connector for low temperature range (< -65°C) 2) High density, high frequency interconnects/connector from Ka to W band targeting active antenna RF front-end 3) Solderless board to board connector (DC and RF) 4) Solderless board to board connector for high data rate applications, radiation-tolerant, blind-mate connector ≥56 Gbps according to different architecture standards (e.g. VITA, OpenVPX) For all above connectors' developments, the project should envisage the following activities: • Within the first 3 months, the project should plan a market and requirement analysis, with primarily focus on all relevant EU space missions (current and future needs) e.g. Galileo, EGNOS, Copernicus, SST, IRIS[2]. The requirement assessment is expected to be included in a dedicated deliverable. The content will be used for complementing and further elaborating the high level requirements reported above • Design and manufacturing • Assembly, electrical testing and reliability assessment • Formal space qualification
Estimated Initial TRL:	3
Target TRL	5-6
Applicable Mission Class(es)	SatCom, EO and Navigation
Remarks / Notes	The reference TRL definition is the ISO Standard 16290. As this development is expected to achieve a full space qualification, applicants are reminded that the Work Programme has specific provisions that must be satisfied (e.g.

	submission of the qualification data pack to the granting authority, …)

3.1.4 ADVANCED PACKAGES

Expected Technology Development	The development of advanced organic substrates with embedded silicon or glass interposer is a crucial step towards enabling the next generation of space electronics. The goal of this development action is to design, manufacture, and test organic substrates based on embedded silicon or glass interposer with very fine line spacing (below 10 µm, goal 5 µm) for very high-density integration, targeting space applications. This activity will provide a significant boost to the EU space industry, enabling the development of more powerful, compact, and reliable electronic systems for space missions. This packaging technology is considered an enabler for the next EU space complex devices based on chiplets e.g. FPGAs, Microprocessors, SiP which integration is expected to take place with a smaller form factor, reducing mass and power consumption. The expected activity should cover the following major steps: 1) Material selection and characterization: Identify and characterize suitable organic materials for the substrate, as well as silicon or glass materials for the interposer, ensuring compatibility and reliability in space environments 2) Design and simulation: Develop and simulate the architecture of the organic substrate with embedded silicon or glass interposer, considering the specific requirements of space applications e.g. thermal stability, and mechanical robustness 3) Fabrication and assembly: Develop and demonstrate the fabrication and assembly processes for the organic substrate with embedded interposer, including the deposition of thin films, patterning, and bonding techniques 4) Testing and validation: Perform thorough testing and validation of the developed substrates, including

	electrical, thermal, and mechanical characterization, as well as reliability assessment During the first three months of the project a market and requirement analysis, with primarily focus on relevant EU space missions (e.g. Galileo, EGNOS, Copernicus, SST, IRIS^2) in a form of deliverable should be planned. The content will be used to iterate the preliminary requirements.
Estimated Initial TRL:	3-4
Target TRL	6-7
Applicable Mission Class(es)	SatCom, EO and Navigation
Remarks / Notes	The reference TRL definition is the ISO Standard 16290.

4 Space Critical Equipment for EU non-dependence

4.1 Navigation Technologies

4.1.1 CHIP SCALE ATOMIC CLOCKS

Expected Technology Development	The activity should focus on the development of precise clocks for navigation and timing applications. In particular, Chip Scale Atomic Clocks (CSAC) for ground and space segment. Space qualified CSACs have been demonstrated and are currently available and produced outside the EU. They are particularly relevant for responding to promising Space use-case, for example satellite synchronization in large LEO telecom constellations. In the last decade CSACs have found also many civilian applications; therefore synergies are expected to take place and to be exploited between terrestrial and space market throughout this development. The final EU based CSAC is expected to meet the following requirements: • Power consumption < 100mW • Volume < 15 cm^3 • Frequency Stability: o Short-term,

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ADEV of at least 1×10^{-11}/1000s
ADEV preferably < 3×10^{-12}/100.000s

Aging < 3×10^{-10} monthly

Galileo and GPS signal compatible
Radiation tolerance:

TID ≥ 30 krad
SEE ≥LET 62 MeV*cm2 /mg

Storage temperature -55 C to 85 C
Operative temperature -40 C to 85 C

The relevant technology for achieving the above mentioned requirements should be selected with the objective of reducing and optimizing the overall CSAC dimensions (volume) and power consumption. Coherent population trapping (CPT) technology could represent a suitable choice, however a comprehensive assessment and technology evaluation should take place at the beginning of the project. The final architectural decision is expected to be taken within the first three months of the project.
Additionally, within the same time frame, the project is expected to undertake a market and requirement analysis, with primarily, but not exclusively, focus on relevant EU space missions (current and future needs) and a dedicated project deliverable should be planned. The content will be used for confirming, discussing and, if relevant, tuning the requirements.
The final product is expected to undergo a full space evaluation proving suitability for space environmental conditions.
The expected CSAC should be developed in a cost-effective manner to minimize the cost per unit. It is expected that the proposal explains the feasibility of the cost reduction and contains an estimation compared to the current market alternatives.
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<tr><td>Estimated Initial TRL</td><td>4</td></tr>
<tr><td>Target TRL</td><td>6</td></tr>
<tr><td>Applicable Mission Class(es)</td><td>Telecommunications, Navigation</td></tr>
<tr><td>Remarks / Notes</td><td>It is recommended to target a formal space qualification.
The reference TRL definition is the ISO Standard 16290.
Applicants are reminded that the Work Programme has specific provisions that must be satisfied (e.g. submission of</td></tr>
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	the evaluation/qualification data pack to the granting authority, EU flag engraving on the package)

4.1 Technologies for Energy

4.1.1 SOLAR CELLS

Expected Technology Development	The activity should focus on the design, development, manufacture and space evaluation for high efficiency solar cells as well as increasing the manufacturing capacity in EU. The targeted solar cells should exceed the performance offered by current products on the EU market.
	
	Currently, in EU there are available solar cells targeting space applications with demonstrated efficiency in the order of 31% and based on triple-junction technology (GaInP/GaAs/Ge). The objective of this development is to increase the efficiency performance to accommodate needs coming from new and future EU Space missions (more and more energy hungry). This development should pay particular attention to provide highest performance values at End of Life (EOL) therefore considering expected degradation of the solar cells due to radiation effects.
	
	The final EU based solar cells are expected to meet the following requirements:
	
	• Efficiency target for BOL and EOL (1MeV electrons,1E15cm-2) achieved together:
	    o > 33% BOL
	    o > 30% EOL
	
	The activity is expected to be broken down in the following major steps:
	
	1) Undertaking a market and requirement analysis, with primarily, but not exclusively, focus on relevant EU space missions (current and future needs and target applications in LEO and MEO) and a dedicated project deliverable should be planned.
	
	2) Identification of optimised solar cell structures with the objective of improving the efficiency figure, without compromising the radiation robustness and ensuring that the device architecture could rely on a stable and reproducible process.

	3) Development of the solar cell structure, or optimisation of existing solar cell, by implementing at least 2 process runs 4) Characterization of test samples against expected electrical and environmental performance for each process run 5) Space evaluation with extended reliability and representative environmental conditions tests (at least for a representative solar cell population responding to the last process run) A dedicated action should be undertaken within this development for contributing to the increase of the solar cells manufacturing capacity in the EU. This could include for example scaling up existing production lines supporting the semiconductor process relevant for this development. The solar cell process shall be oriented toward an effective cost/W ratio.
Estimated Initial TRL	3-4
Target TRL	5-6
Applicable Mission Class(es)	Telecommunications, Navigation, EO
Remarks / Notes	It is recommended to target a formal space qualification. The reference TRL definition is the ISO Standard 16290.